

PERFORMANCE SPECIFICATION

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED
(TOTAL DOSE AND SINGLE EVENT EFFECTS) TRANSISTOR, N-CHANNEL
SILICON TYPES 2N7512, 2N7513, AND 2N7514
JANTXVD, R AND JANSJ, R

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE) characterization), power transistor intended for use in high density power switching applications. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1, TO-257.

1.3 Maximum ratings. $T_A = +25^\circ\text{C}$, unless otherwise specified.

Type	P_T $T_C = +25^\circ\text{C}$	V_{DS}	V_{DG}	V_{GS}	I_{D1} (1) $T_C = +25^\circ\text{C}$	I_{D2} (1) $T_C = +100^\circ\text{C}$	I_S (1)	I_{DM}	T_J and T_{STG}	V_{ISO} 70,000 ft. altitude
	<u>W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>°C</u>	<u>V dc</u>
2N7512	56 (2)	100	100	± 30	16	15	16	64	-55	N/A
2N7513	56 (2)	200	200	± 30	14	9	14	40	to	N/A
2N7514	50 (3)	250	250	± 30	11	7	11	32	+150	250

(1) $I_D = ((T_{jmax} - T_C) / ((R_{\theta JC}) \times (r_{DS(on)} \text{ at } T_{jmax})))^{1/2}$.

(2) Derate linearly $0.45 \text{ W}/^\circ\text{C}$ for $T_C > +25^\circ\text{C}$; $P_T = (T_{jmax} - T_C) / R_{\theta JC}$.

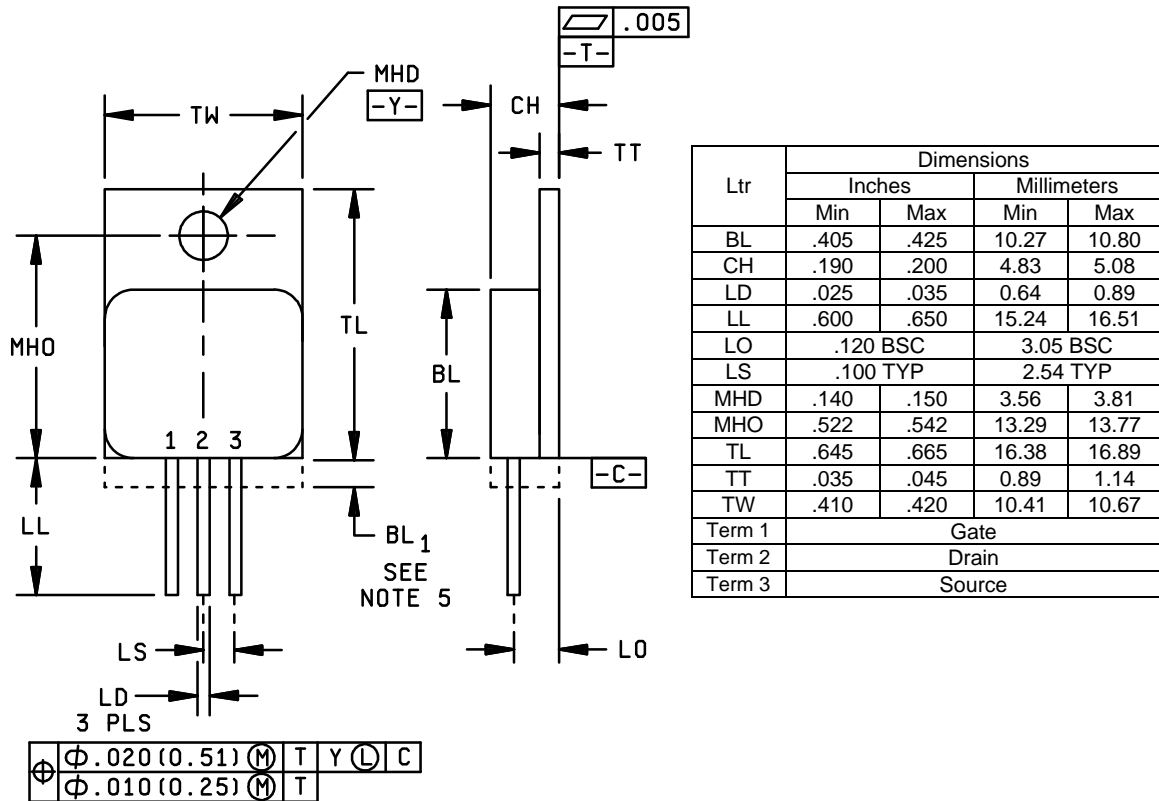
(3) Derate linearly $0.40 \text{ W}/^\circ\text{C}$ for $T_C > +25^\circ\text{C}$; $P_T = (T_{jmax} - T_C) / R_{\theta JC}$.

1.4 Primary electrical characteristics at $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0 \text{ mA dc}$	$V_{GS(TH)1}$ $V_{DS} = V_{GS}$ $I_D = 1.0 \text{ mA dc}$	Max I_{DSS1} $V_{GS} = 0$ $V_{GS} = 80\%$ of rated V_{DS}	Max $r_{DS(on)}$ (1) $V_{GS} = 12 \text{ V}$		$R_{\theta JC}$ Max	I_{AS}
				$T_J = +25^\circ\text{C}$ at I_{D2}	$T_J = +125^\circ\text{C}$ at I_{D2}		
	<u>V dc</u>	<u>V dc</u> Min Max 2.0 4.5	<u>$\mu\text{A dc}$</u>	<u>Ω</u>	<u>Ω</u>	<u>°C/W</u>	<u>A (pk)</u>
2N7512	100		25	0.054	0.090	2.2	54
2N7513	200			0.155	0.310		36
2N7514	250			0.230	0.449		11

(1) Pulsed (see 4.5.1).

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Defense Supply Center, Columbus, ATTN: DSCC/VAC, Post Office Box 3990, Columbus, OH 43216-5000, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.



NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. All terminals are isolated from case.
4. The preferred measurements used herein are the inch units. This transistor was designed using inch-pound units of measurement. In case of conflicts between the metric and inch-pound units, the inch-pound units shall be the rule.
5. This area is for the lead feed-thru eyelets (configuration is optional, but will not extend beyond this zone).
6. Die to base is BeO isolated, terminals to case ceramic (AL₂O₃) isolated.
7. In accordance with ANSI Y14.5M, diameters are equivalent to ϕ x symbology.
8. Dimension LD applies to base metal only.

FIGURE 1. Physical dimensions (similar to TO-257).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

STANDARD

DEPARTMENT OF DEFENSE

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Document Automation and Production Services (DAPS), Building 4D (DPM-DODSSP), 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The requirements for acquiring the product described herein shall consist of this document and MIL-PRF-19500.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1.

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be group A as specified herein.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container.

3.8 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.8.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended:

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq$ or 100 k Ω , whenever bias voltage is applied drain to source.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of Inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500. Alternate flow is allowed for qualification inspection in accordance with figure 4 of MIL-PRF-19500.

4.2.1 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IX of MIL-PRF-19500, and table III herein. Electrical measurements (end-points) shall be in accordance with table I, group A, subgroup 2 herein.

4.2.1.1 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. See the design safe operation area figures herein. Electrical measurements (end-points) shall be in accordance with table I, group A, subgroup 2 herein.

4.3 Screening. Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurement	
	JANS	JANTXV
(1)	Method 3470 E _{AS} test (see 4.5.4)	Method 3470 E _{AS} test (see 4.5.4)
(1)	Method 3161 (see 4.5.3)	Method 3161 (see 4.5.3)
(1)	Gate stress test (see 4.5.5)	Gate stress test (see 4.5.5)
(2)	Subgroup 2 of table I herein	Subgroup 2 of table I herein
9	I _{GSS} , I _{DSS1} as a minimum	I _{GSS} , I _{DSS1} as a minimum
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(ON)} , V _{GS(TH)} Subgroup 2 of table I herein. ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±25 μA dc or ±100 percent of initial value, whichever is greater.	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(ON)} , V _{GS(TH)} subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A, 240 hours minimum.	Method 1042 of MIL-STD-750, test condition A, 160 hours minimum.
13	Subgroups 2 and 3 of table I herein ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±25 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(ON)1} = ±20 percent of initial value. ΔV _{GS(TH)1} = ±20 percent of initial value.	Subgroup 2 table I herein ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±25 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(ON)1} = ±20 percent of initial value. ΔV _{GS(TH)1} = ±20 percent of initial value.

- (1) Shall be performed anytime before screen 10.
- (2) Shall be performed after E_{AS} test, method 3161, and gate stress test.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500. Alternate flow is allowed for quality conformance inspection in accordance with figure 4 of MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in tables VIa (JANS) and VIb (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and 4.4.2.1 and 4.4.2.2 herein. Electrical measurements (end-points) shall be in accordance with table I, group A, subgroup 2 herein. Delta V_{SD} measurements shall be in accordance with table IV herein.

4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition F or G, 100 cycles.
B4	1042	Intermittent operation life, condition D, 2,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. T_{on} = 30 seconds minimum.
B5	1042	Accelerated steady-state reverse bias, condition A.
B5	1042	Accelerated steady-state gate bias, condition B.
B6	3161	Thermal resistance, see 4.5.2.

4.4.2.2 Group B inspection, table VIb (JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1042	Intermittent operation life, condition D, 2,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. T_{on} = 30 seconds minimum.
B5	3161	Thermal resistance, see 4.5.2.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, group A, subgroup 2 herein. Delta V_{SD} measurements shall be in accordance with table IV herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
2	2036	Terminal strength, test condition A, weight = 10 pounds, t = 15 seconds.
6	1042	Intermittent operation life, condition D, 6,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. T_{on} = 30 seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table VIII of MIL-PRF-19500 and table II herein.

4.4.4.1 Design parameters. Not tested on a per lot basis. Design shall be such that the devices shall be capable of meeting the requirements of SEE safe operating area graphs herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. Thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750. The maximum limit of $R_{\theta JC} = 2.2^{\circ}\text{C/W}$. The following parameters shall apply:

- a. Measuring current (I_M)..... 10 mA.
- b. Drain heating current (I_H)..... 1 A.
- c. Heating time (t_H)..... Steady-state (see method 3161 of MIL-STD-750).
- d. Drain-source heating voltage (V_H)..... 25 V.
- e. Measurement time delay (t_{MD})..... 30 to 60 μs .
- f. Sample window time (t_{SW})..... 10 μs maximum.

4.5.3 Thermal response (V_{SD} measurement). The delta V_{SD} measurement shall be performed in accordance with method 3161 of MIL-STD-750. The delta V_{SD} conditions (I_H and V_H) and maximum limit shall be derived by each vendor from the thermal response curves (see figure 2) and shall be specified in the certificate of conformance prior to qualification. The following parameter measurements shall apply:

- a. Measuring current (I_M)..... 10 mA.
- b. Drain heating current (I_H)..... 1 A.
- c. Heating time (t_H)..... 100 ms.
- d. Drain-source heating voltage (V_H)..... 25 V.
- e. Measurement time delay (t_{MD})..... 30 - 60 μs .
- f. Sample window time (t_{SW})..... 10 μs maximum.

4.5.4 Single pulse avalanche energy (E_{AS}).

- a. I_{AS} shall be as specified in 1.4 herein.
- b. $L = 0.1 \text{ mH}$.
- c. Gate to source resistor ($25 \Omega \leq R_{GS} \leq 200\Omega$).
- d. $E_{AS} = 1/2 L I_{AS}^2$.
- e. $V_{DD} = 50 \text{ V to } 150 \text{ V dc}$.
- f. Initial junction temperature = $+25^{\circ}\text{C}$, -5°C , $+10^{\circ}\text{C}$.

4.5.5 Gate stress test.

- a. $V_{GS} = 45 \text{ V}$.
- b. $t = 250 \mu\text{s}$, minimum.

TABLE I. Group A inspection

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Breakdown voltage drain to source	3407	$V_{GS} = 0V$, $I_D = 1 \text{ mA dc}$, bias condition C	$V_{(BR)DSS}$	100		V dc
2N7512				200		V dc
2N7513				250		V dc
2N7514						
Gate to source voltage (threshold)	3403	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA dc}$	$V_{GS(TH)1}$	2.0	4.5	V dc
Gate current	3411	$V_{GS} = \pm 30 \text{ V dc}$, bias condition C, $V_{DS} = 0V$	I_{GSS1}		± 100	nA dc
Drain current	3413	$V_{GS} = 0V \text{ dc}$, bias condition C, $V_{DS} = 80 \text{ percent of rated } V_{DS}$	I_{DSS1}		25	$\mu A \text{ dc}$
Static drain to source "ON" state resistance	3421	$V_{GS} = 12V \text{ dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$		0.054	Ω
2N7512					0.155	Ω
2N7513					0.230	Ω
2N7514						
Static drain to source "ON" state resistance	3405	$V_{GS} = 12V \text{ dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$V_{DS(ON)}$		0.880	V dc
2N7512					2.31	V dc
2N7513					2.64	V dc
2N7514						
Forward voltage	4011	$V_{GS} = 0V \text{ dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}		1.2	V dc
<u>Subgroup 3</u>						
High temperature operation		$T_C = T_J = +125^\circ C$				
Gate current	3411	$V_{GS} = \pm 30V \text{ dc}$, bias condition C, $V_{DS} = 0 \text{ V}$	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0V \text{ dc}$, bias condition C, $V_{DS} = 80 \text{ percent of rated } V_{DS}$	I_{DSS2}		0.250	mA dc
Static drain to source "ON" state resistance	3421	$V_{GS} = 12V \text{ dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$r_{DS(ON)2}$		0.090	Ω
2N7512					0.310	Ω
2N7513					0.449	Ω
2N7514						

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3 - continued</u>						
Gate to source voltage (threshold)	3403	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA dc}$	$V_{GS(TH)2}$	1.0		V dc
Low temperature operation		$T_C = T_J = -55^{\circ}\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA dc}$	$V_{GS(TH)3}$		5.5	V dc
<u>Subgroup 4</u>						
Switching time test	3472	$I_D = I_{D1}$, $V_{GS} = 12 \text{ V dc}$, $R_G = 7.5 \Omega$, $V_{DD} = 50 \text{ percent of rated } V_{DS}$				
Turn-on delay time			$t_{D(on)}$			
2N7512					20	ns
2N7513					20	ns
2N7514					20	ns
Rise Time			t_R			
2N7512					40	ns
2N7513					40	ns
2N7514					40	ns
Turn-off delay time			$t_{D(off)}$			
2N7512					35	ns
2N7513					35	ns
2N7514					35	ns
Fall time			t_f			
2N7512					15	ns
2N7513					15	ns
2N7514					30	ns
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 3, $t_p = 10 \text{ ms min.}$ $V_{DS} = 80 \text{ percent of max. rated } V_{DS}$ ($V_{DS} \leq 200 \text{ V}$)				
Electrical measurements		See table I, group A, subgroup 2 herein.				
<u>Subgroup 6</u>						
Not applicable						

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 7</u>						
Gate charge	3471	Condition A or B	$Q_{G(ON)}$			
On-state gate charge						
2N7512					35	nC
2N7513					28	nC
2N7514					28	nC
Gate to source charge			Q_{GS}			
2N7512					13	nC
2N7513					12	nC
2N7514					12	nC
Gate to drain charge			Q_{GD}			
2N7512					12	nC
2N7513					10	nC
2N7514					10	nC
Reverse recovery time	3473	$di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq 50 \text{ V}$, $I_D = I_{D1}$	t_{rr}			
2N7512					180	ns
2N7513					220	ns
2N7514					410	ns

1/ For sampling plan, see MIL-PRF-19500.

TABLE II. Group D inspection.

Inspection <u>1/ 2/ 3/ 4/ 5/</u>	MIL-STD-750		Symbol	Pre-irradiation limits		Post irradiation limits		Units
	Method	Conditions		Min.	Max.	Min.	Max.	
<u>Subgroup 1</u>								
Not applicable								
<u>Subgroup 2</u>		$T_C = +25^{\circ}\text{C}$						
Steady state total dose irradiation (V_{GS} bias)	1019	$V_{GS} = 12\text{V}, V_{DS} = 0\text{V}$						
Steady state total dose irradiation (V_{DS} bias)	1019	$V_{GS} = 0\text{V}, V_{DS} = 80$ percent of rated V_{DS}						
Breakdown voltage drain to source 2N7512 2N7513 2N7514	3407	$V_{GS} = 0\text{V}, I_D = 1\text{ mA}$ dc, bias condition C	$V_{(BR)DSS}$	100 200 250		100 200 250		V dc V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$ dc	$V_{GS(TH)1}$	2.0	4.5	2.0	4.5	V dc
Gate current	3411	$V_{GS} = \pm 30\text{V}$ dc, $V_{DS} = 0\text{V}$, bias condition C	I_{GSS1}		± 100		± 100	nA dc
Drain current	3413	$V_{GS} = 0\text{V}, V_{DS} = 80$ percent of rated V_{DS} , bias condition C	I_{DSS1}		25		25	μA dc
Static drain to source "ON"-state resistance 2N7512 2N7513 2N7514	3421	$V_{GS} = 12\text{V}$ dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$		0.054 1.155 0.230		0.054 1.155 0.230	Ω Ω Ω
Static drain to source "ON"-state voltage 2N7512 2N7513 2N7514	3405	$V_{GS} = 12\text{V}$ dc, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$V_{DS(ON)}$		0.88 2.31 2.64		0.88 2.31 2.64	V dc V dc V dc

1/ For sampling plan see MIL-PRF-19500.

2/ Electrical specifications are for 'D' and 'R' rad levels.

3/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other detail specification utilizing the same die design.

4/ Separate samples shall be pulled for each bias.

5/ At the manufacturer's option, group D samples need not be subjected to all the screening tests, but shall be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

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TABLE III. Group E inspection (all quality levels) - for qualification only.

Inspection 1/	MIL-STD-750		Qualification and large lot conformance inspection
	Method	Conditions	
<u>Subgroup 1</u>			12 devices c = 0
Temperature cycling (air to air)	1051	Test condition F or G, 500 cycles	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I, group A, subgroup 2 herein.	
<u>Subgroup 2 2/</u>			12 devices c = 0
Steady-state gate bias	1042	Test condition B; 1,000 hours	
Electrical measurements		See table I, group A, subgroup 2 herein.	
Steady-state reverse bias	1042	Test condition A; 1,000 hours	
Electrical measurements		See table I, group A, subgroup 2 herein.	
<u>Subgroup 3</u>			
Not applicable			
<u>Subgroup 4</u>			22 devices c = 0
Thermal resistance	3161	$R_{\theta JC} = 2.2^{\circ}\text{C/W}$ maximum. See 4.5.2.	
<u>Subgroup 5</u>			15 devices c = 0
Barometric pressure test (not required for $V_{BR(DSS)} \leq 200\text{ V}$) 2N7514	1001	Test condition C $V_{DS} = 250\text{ V}; I_{(ISO)} < 0.25\text{ mA}$	

See footnotes at end of table.

TABLE III. Group E inspection (all quality levels) - for qualification only - Continued.

Inspection	MIL-STD-750		Qualification and large lot conformance inspection
	Method	Conditions	
<u>Subgroup 6</u> Electrical measurements <u>3/</u> SEE testing <u>4/</u> 2N7512 2N7513 2N7514	1080	<p>See group A, table I, subgroup 2 herein, I_{GSS1} and I_{DSS1} tests.</p> <p>Fluence = $3e5 \pm 20$ percent ions/cm² Flux = $5e3$ to $2e4$ ions/cm²sec Beam energy = 260 to 360 MeV Temperature = $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$</p> <p>LET = 36 to 40 MeV-cm²/mg Ion range = 35 to 40 microns Insitu bias conditions: $V_{DS} = 100$ V and $V_{GS} = -10$ V</p> <p>LET = 56 to 60 MeV-cm²/mg Ion range = 30 to 35 microns Insitu bias conditions: $V_{DS} = 100$ V and $V_{GS} = -5$ V $V_{DS} = 50$ V and $V_{GS} = -8$ V</p> <p>LET = 80 to 84 MeV-cm²/mg Ion range = 25 to 30 microns Insitu bias conditions: $V_{DS} = 80$ V and $V_{GS} = 0$ V $V_{DS} = 50$ V and $V_{GS} = -5$ V</p> <p>LET = 36 to 40 MeV-cm²/mg Ion range = 35 to 40 microns Insitu bias conditions: $V_{DS} = 200$ V and $V_{GS} = -20$ V</p> <p>LET = 56 to 60 MeV-cm²/mg Ion range = 30 to 35 microns Insitu bias conditions: $V_{DS} = 200$ V and $V_{GS} = -10$ V</p> <p>LET = 80 to 84 MeV-cm²/mg Ion range = 25 to 30 microns Insitu bias conditions: $V_{DS} = 160$ V and $V_{GS} = -5$ V $V_{DS} = 120$ V and $V_{GS} = -10$ V</p> <p>LET = 36 to 40 MeV-cm²/mg Ion range = 35 to 40 microns Insitu bias conditions: $V_{DS} = 250$ V and $V_{GS} = -20$ V</p> <p>LET = 56 to 60 MeV-cm²/mg Ion range = 30 to 35 microns Insitu bias conditions: $V_{DS} = 250$ V and $V_{GS} = -10$ V</p> <p>LET = 80 to 84 MeV-cm²/mg Ion range = 25 to 30 microns Insitu bias conditions: $V_{DS} = 200$ V and $V_{GS} = -5$ V $V_{DS} = 150$ V and $V_{GS} = -10$ V</p>	3 devices <u>5/</u> c = 0

TABLE III. Group E inspection (all quality levels) - for qualification only - Continued.

Inspection <u>1/</u>	MIL-STD-750		Qualification and large lot conformance inspection
	Method	Conditions	
<u>Subgroup 6</u> Electrical measurements <u>3/</u> ESD (Electrostatic Discharge Protection)	1020	See group A, table I, subgroup 2 herein, I_{GSS1} and I_{DSS1} tests.	3 devices $c = 0$

- 1/ Group E qualification of SEE testing may be performed prior to lot formation. Wafers qualified to these group E QCI requirements may be used for any other performance specification utilizing the same die design.
- 2/ A separate sample for each test may be pulled.
- 3/ As a minimum, gate to source leakages and drain to source leakage are to be examined to verify the electrical performance of the DUT prior to and after test. At the manufacturer's option, the remaining tests in table I, group A, subgroup 2 may be performed.
- 4/ Devices passing a given combination of drain and gate voltage for an LET of 80 to 84 MeV-cm²/mg qualify the same conditions for an LET of 56 to 60 MeV-cm²/mg or an LET of 36 to 40 MeV-cm²/mg.
- 5/ This sampling plan applies to each bias condition specified.

TABLE IV. Group B, C and E delta measurements

Step	Inspection <u>1/</u> <u>2/</u>	MIL-STD-750		Symbol	Limits		Units
		Method	Conditions		Min	Max	
1.	Thermal response	3161	See 4.5.3	ΔV_{SD}		125	mV

- 1/ The delta measurements for group B, table VIa (JANS) of MIL-PRF-19500 shall be step 1 above and shall be in subgroup 4.
- 2/ The delta measurements for group C, table VII of MIL-PRF-19500 shall be step 1 above and shall be in subgroup 6.

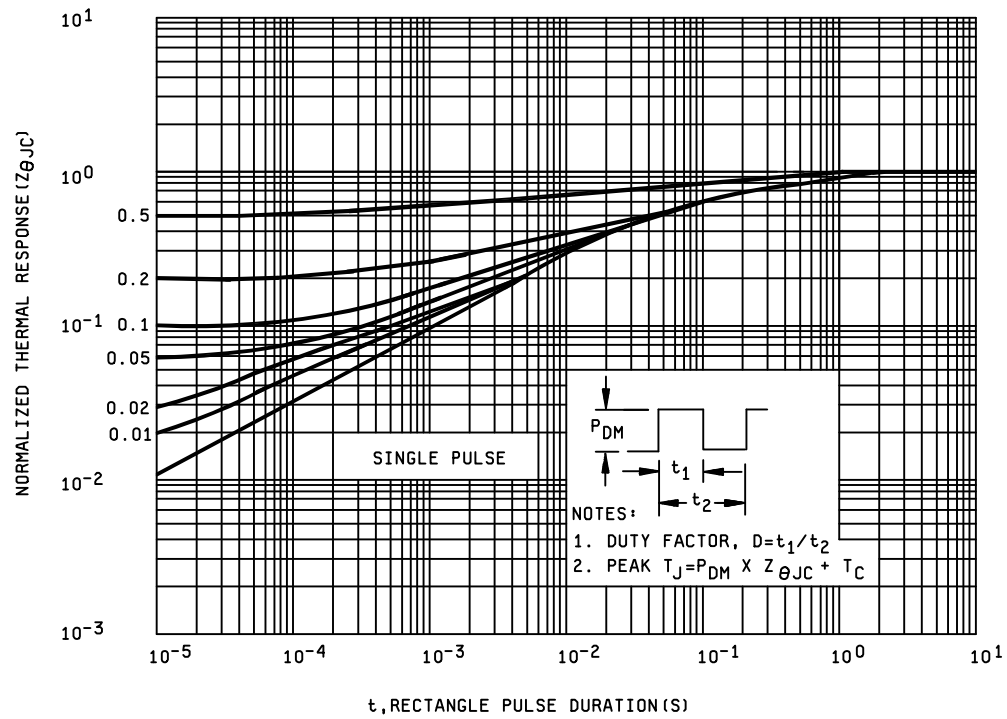


FIGURE 2. Thermal response curves.

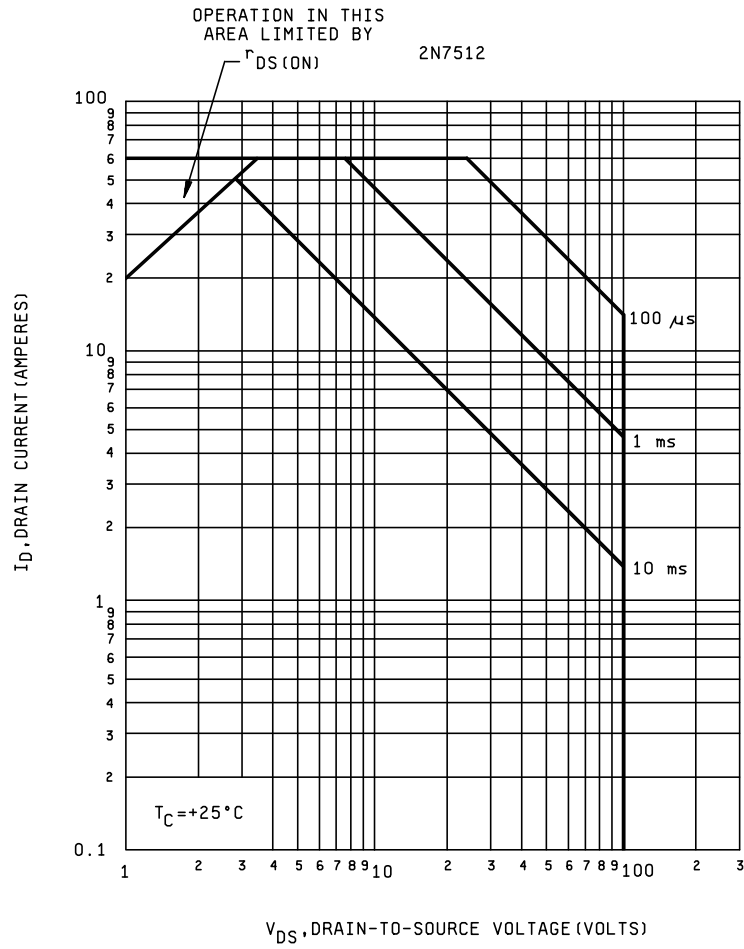
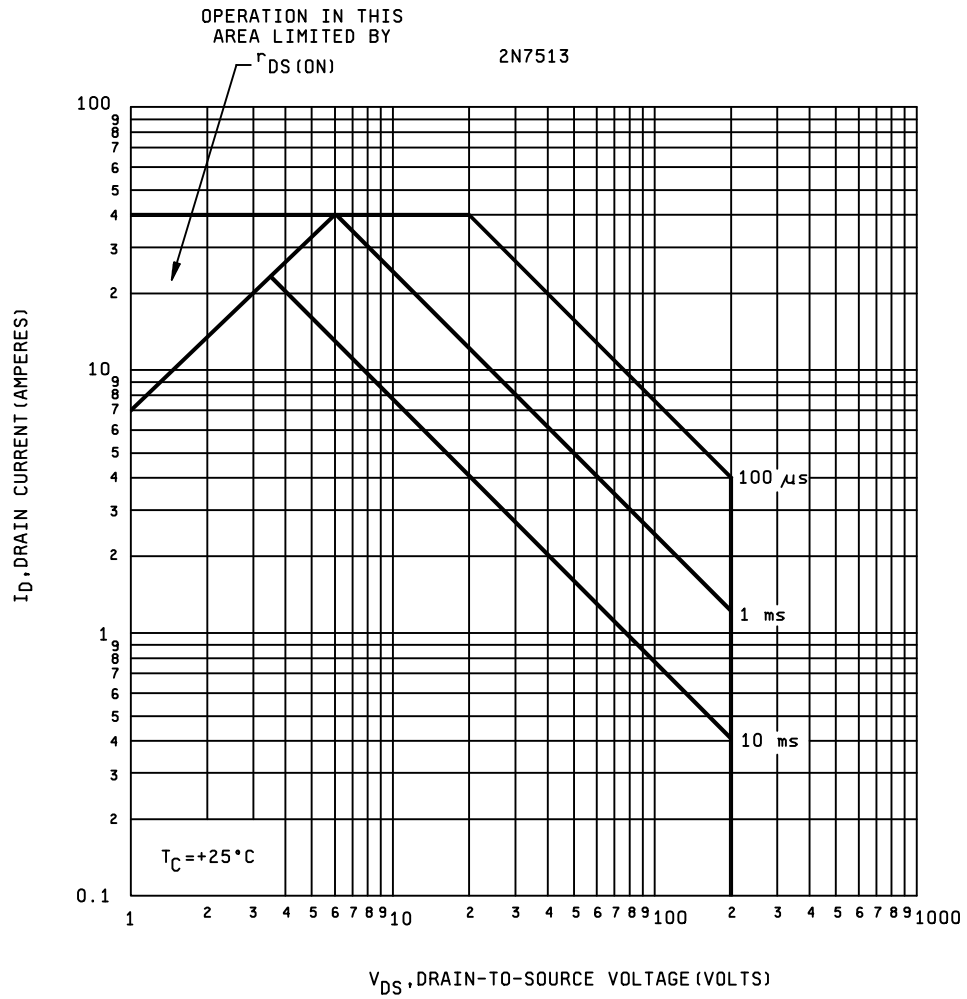


FIGURE 3. Safe operating area graphs.

FIGURE 3. Safe operating area graphs - Continued.

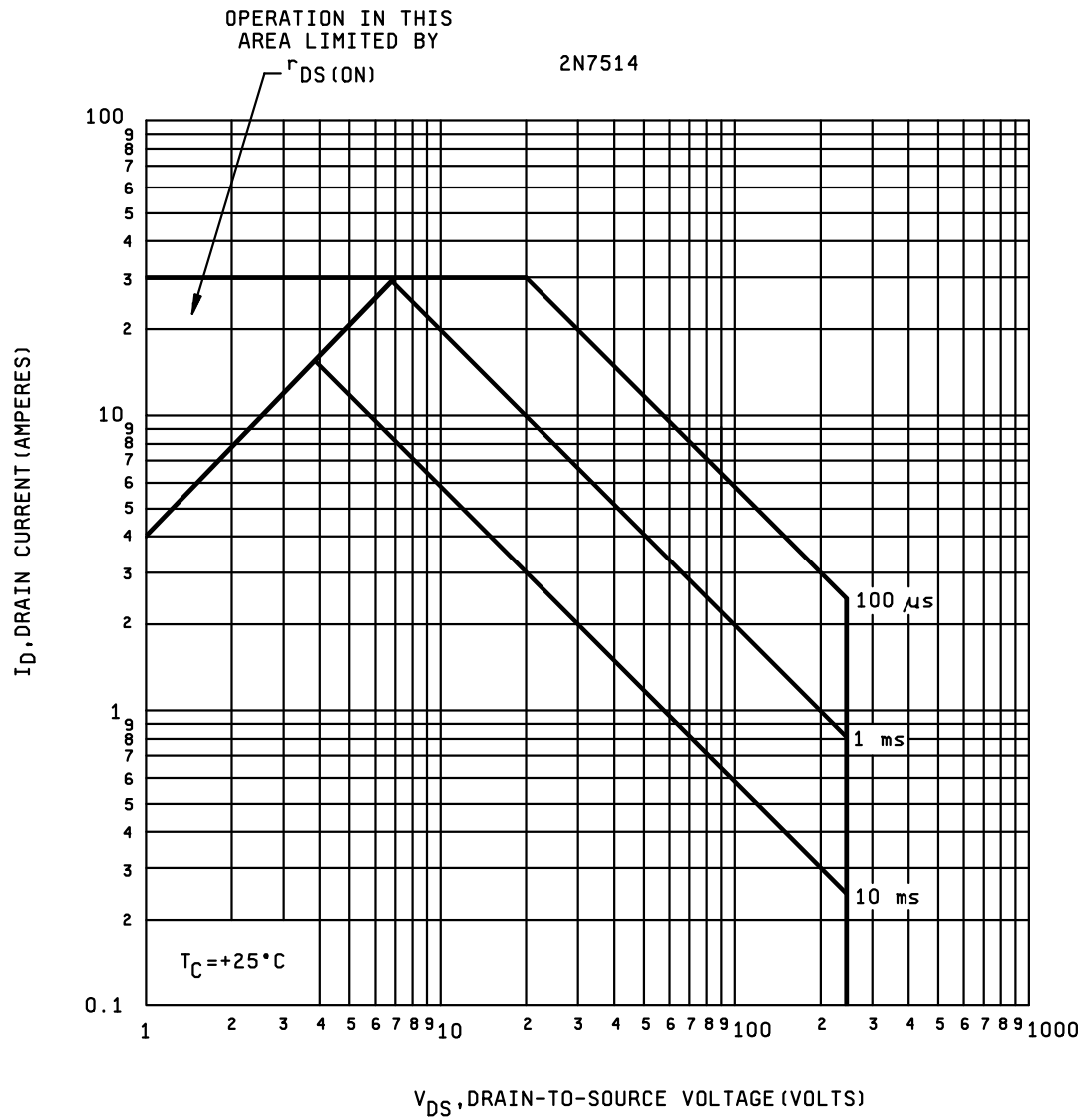


FIGURE 3. Safe operating area graphs - Continued.

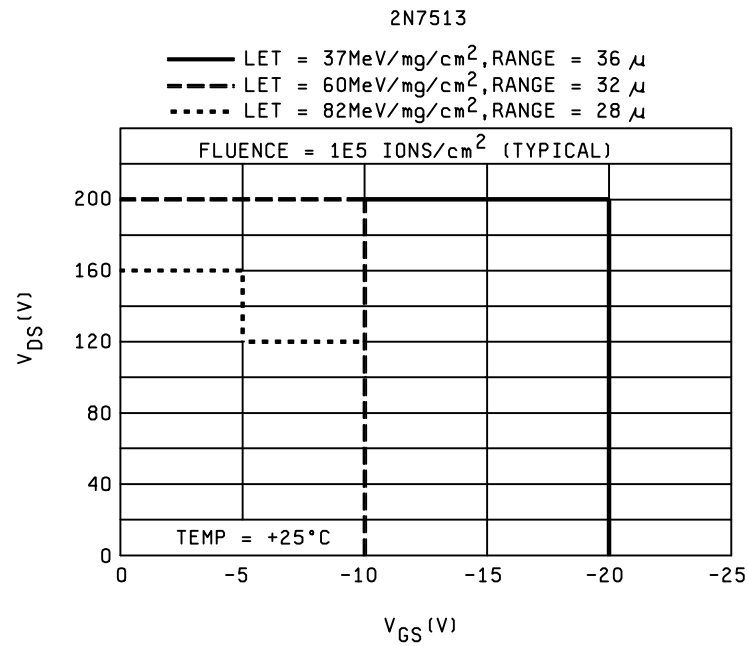
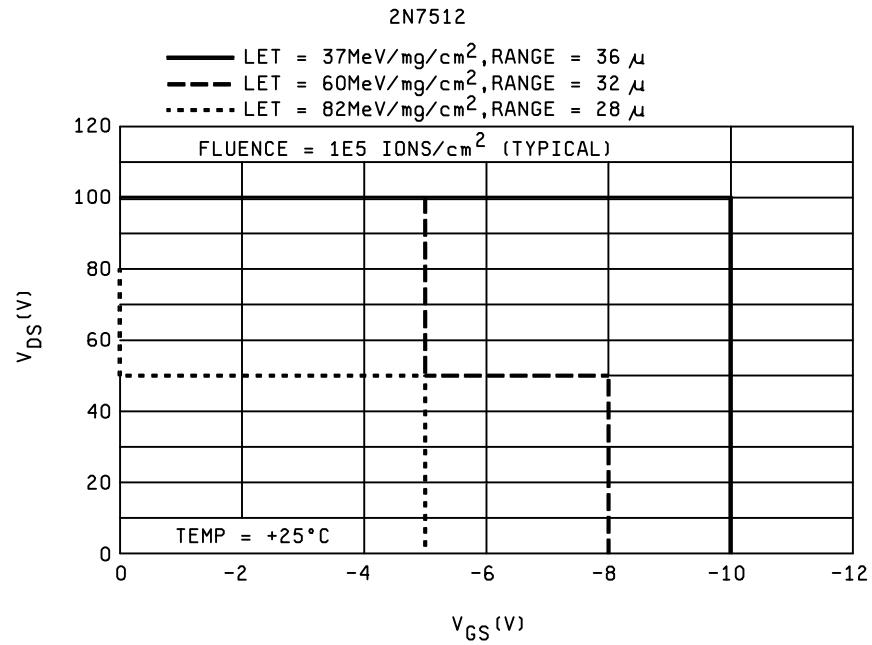
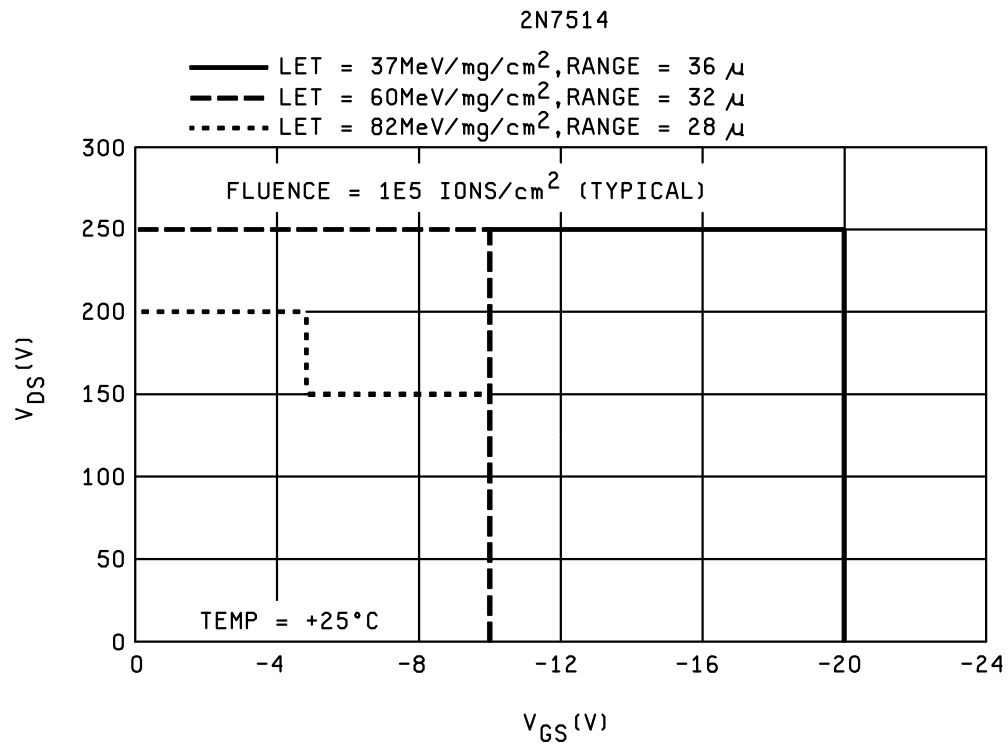


FIGURE 4. SEE safe operating area graphs.

FIGURE 4. SEE safe operating area graphs. - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department or Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. The acquisition requirements are as specified in MIL-PRF-19500.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers' List (QML) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43216-5000.

6.4 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N
FSGS130	2N7512
FSGS230	2N7513
FSGS234	2N7514

Custodians:
 Army - CR
 Navy - EC
 Air Force - 11
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC

(Project 5961-2413)

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MIL-PRF-19500/689

2. DOCUMENT DATE
28 February 2001

3. DOCUMENT TITLE

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED (TOTAL DOSE AND SINGLE EVENT EFFECTS)
TRANSISTOR, N-CHANNEL SILICON TYPES 2N7512, 2N7513, AND 2N7514 JANTXVD, R AND JANSJ, R

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

5. REASON FOR RECOMMENDATION

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8. PREPARING ACTIVITY

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